

Microelectronics (MNV) - Summary

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1 Introduction:

Circuit types:

Digital circuits:

- Large Signal-to-Noise ratio
- Simple storage
- Easy technology
- Good design automation

Analog circuits:

- Amps, mixer ...
- Capacitors, inductors, resistors
- Problems: tolerance, noise, drift
- Low design automation

Mixed signal circuits:

- Combination of digital and analog

Smart power circuits:

- Power Electronics ic's

Smart sensor circuits:

- Combination of sensor. dsp and Power driver

Transistor technologies:

Bipolar:

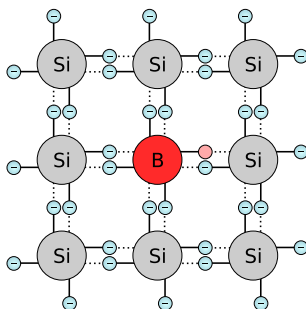
- o Dominant in 70s (TTL)
- + 2-5 times faster than MOS
- + Good for Analog
- Large power consumption
(20 times higher than MOS)
- Big size

CMOS:

- + High integration density
- + Robust
- + no DC power consumption
- + Self-alignment technology process
- + Simple structure
- + Large SNR

2 Doping

P:

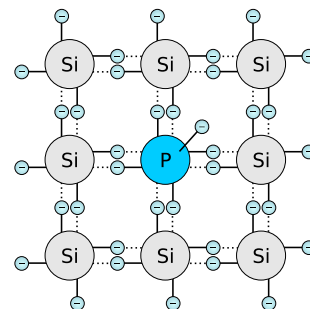


Charge carriers:

Majority: holes

Minority: electrons

N:



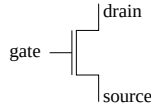
Charge carriers:

Majority: electrons

Minority: holes

3 The MOS Transistor

NMOS:

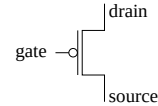


ON State: Gate = '1'

OFF STATE: Gate = '0'

The NMOS transistor is used to switch '0'.

PMOS:

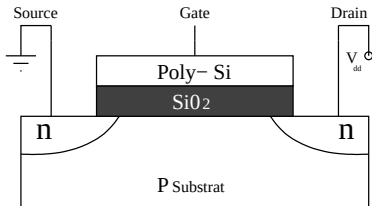


ON State: Gate = '0'

OFF STATE: Gate = '1'

The PMOS transistor is used to switch '1'.

Structure of a MOS Transistor:



- Negative or 0 potential at the gate block the pn-junction
- Positive potential at the gate accumulate electrons from the p substrate below the SiO_2 forming a conductin n-channel between source and drain → "Switch closed"

Three States for the Mosfet:

Accumulation $V_{gs} \leq 0$ Accumulation of holes:

The electrical field draws holes from the p substrat into the channel → no free electrons

Depletion $V_{gs} > 0$ Depletion of holes:

Holes are pushed off from the channel, no free charge carriers. (Negligible current flow between drain and source due to parasitic bipolar transistor [a problem today])

Inversion $V_{gs} > V_{th}$

Electrons from the source are accumulated in the channel forming a conduction inversion layer. The threshold depends on technology and bulk.

MOS Transistor Equations:

Linear: $V_{DS} < V_{GS} - V_{TH}$

Saturation: $V_{DS} > V_{GS} - V_{TH}$

→ The channel is pinched off

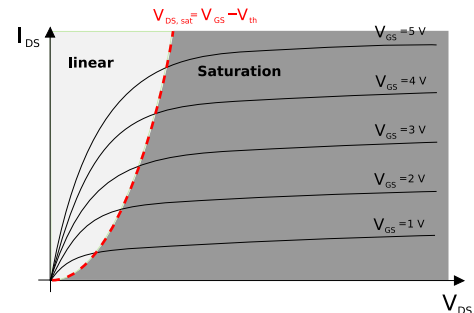
→ current source controlled by V_{GS} .

Long and Short Channel: behavior of I_{DS} , V_{DS} :

Long channel: quadratic

Short channel: linear

Operating Regions



4 Manufacturing

Differences in Modern CMOS Process Technologies:

- Minimum feature size
- Gate oxide thickness
- Number of interconnect layers
- Type of substrat material
- Gate material (alu, polysilicon)
- Method of isolating transistors (locos, sti)
- Type of transistors (nMOS, pMOS, ...)

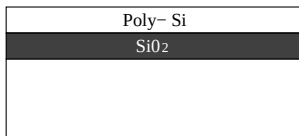
Manufacturing Basics:

- Base material: polysilicon
- Drawn out of rotating pot about 1440 Celsius to a rod-shaped mono crystal (Melt ist enhanced with boron or phosphor → p-substrat, n-substrat)
- Rod is saen into flat wafers and reworked (e.g. polishing)

4.1 Planar Technologies: 4 Basic Steps

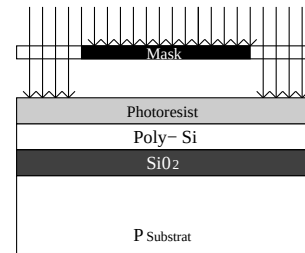
1. Deposition:

Deposition of layers over the complete wafer.
(chemical, thermal oxidation, sputtering...)



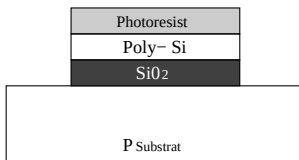
2. Litographie:

- Organic photorisisist
- Exposure of photoresist via mask
- Development and bake



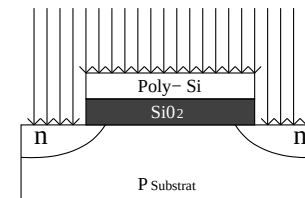
3. Etching:

- Acid etching
- Spin and dry
- Further processing, photoresist removal



4. Doping:

- Self-adjusting process
- Insert Donators in the p-substrat



Trough multiple application of the different single process steps (400 times) the IC grows on wafer.

4.2 Design Rules and Yield

Layout Rules:

Layout rules are the interface between circuit designer and process engineer. (Electronic and geometric constraints.)

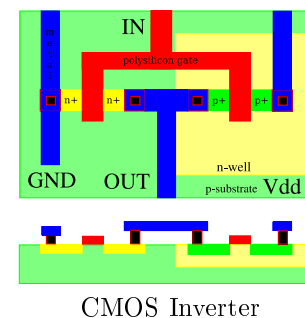
- Minimum width (interruption of wires)
- Minimum spacing (short-circuit)
- Minimum overlap
- Minimum line width

Two Metrics:

μm : absolute value

λ : integer multiple (e.g. min. line width = 2λ)

Example for a Layout:



CMOS Inverter

Yield:

- Area Yield $Y_F = \frac{\text{Working Wafer}}{\text{Total Wafer}}$
 - Chip Yield $Y_B = \frac{\text{Working Chips on Wafer}}{\text{Total Chips on Wafer}}$
 - Assembly Yield $Y_M = \frac{\text{Working Chips in Case}}{\text{Total Chips in Case}}$
 - Test yield $Y_P = \frac{\text{Working Blocks}}{\text{Total Blocks}}$
- $$Y_{Total} = Y_F \cdot Y_B \cdot Y_M \cdot Y_P$$

For Instance: Chip Yield

Particle contamination with diameter smaller than minimal structure can lead to local short-circuits.
→ Redundant circuits on chip which can be activated in defective chips (e.g. DRAM).

$$Y_B \sim 1 - n \cdot A_{dip} \cdot D_0$$

Yield improvement also by Design Manufacturebility (DFM): e.g. Wire spreading

→ Design rules are a compromise between yield (errornous wafer...), size and performance

Packaging:

- After wafer processing test of chips on wafer
- Slicing the wafer into single chips
- Defect free chips are packaged (dip...)
- Bonding techniques (wire bonding, tape...)
- Test of packaged chips

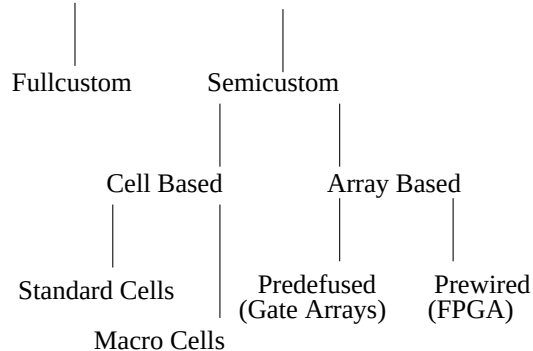
Requirements on a Package:

- Electrical: low parasitics (L,C...)
- Mechanical: reliable and robust
- Thermal: efficient heat removal
- Economical: cheap

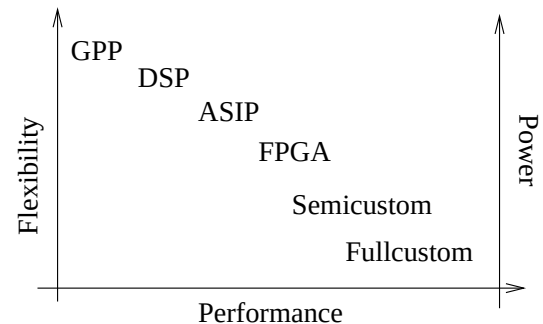
5 Implementation Styles

Overview:

Digital Circuit Implementation Approaches



Differences:



Fullcustom Design:

- Design element *single transistor*
- Circuit and layout design is mostly handwork
- No constraints on design process
- Very compact design, but very limited CAD

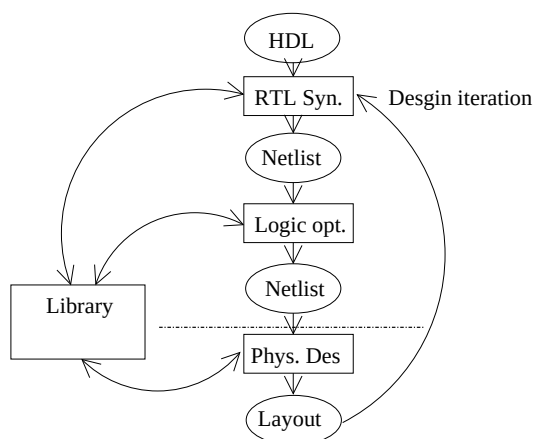
e.g. DRAM, analogue...

Semi Custom

- Cell Based:
 - Standard cells, macrocells (Design element *cell* with predefined functionality, timing and layout structure)
- Array based:
 - Pre-diffused: gate arrays, sea of gates
 - Pre-wired: antifuse based, memory based
- Functional design and layout generation automated
- Technology independent design

5.1 Semi Custom - Cell based:

Library Concept:



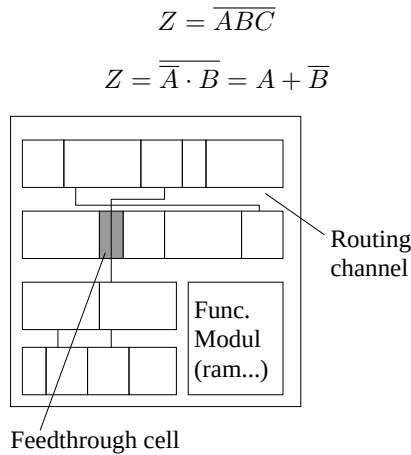
Standard Cells:

- Designed and characterized as a "full custom" design
- High degree of automation (synthesis, place & route, all cells have same height...)

Library Concept for Standard Cells:

- Functional timing, power and electrical behavior are predefined and stored in library
- Typical library contains several hundreds of cells (NAND, NOR, MUX, FF ...) with area-performance and power-optimized cell instances

Examples for Standard Cells:



Hard Macrocells:

- Provide functionality and predetermined phys. design
- Predictable performance and power dissipation
- Dense layout but tech. dependent
- e.g. Memory, Multiplier, embedded processors

Soft Macrocells:

- Physical layout is generated by synthesis for each instance
- Limited predictable performance
- Easy to port to different tech.

5.2 Semi Custom - Array based:

Array Concept:

- Reducing fabrication cost
- Partly or completely prefabricated components
- Late binding implementation (personalization)
- Personalisation by:
 - a) *Metalization* (pre diffused) Gate Arrays
 - b) *Programming* (pre wired) FPGA

Gate Arrays:

- Simplification of std. cells → all cells are identical
- Personalisation only via metallization
- Number of cells rows and wiring channels are fixed

Sea-of-Gates:

- Same as Gate array but cell is a single transistor
- Numbers of rows and channels are not fixed. The chip is covered by transistors and the wires are routed over transistors.

Programmable Prewired Concept:

- Allows personalization of IC's without fabrication steps
- Programming one by the user (VHDL...)
- Less costs for low quantities (<10000)

Programmable Logic Devices:

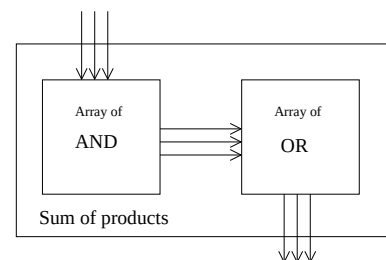
- **PLA/PAL:** Programmable Array Logic (2-Stage-Logic)
- **CPLD:** Complex Programmable Logical Device (PLA+FF for simple sequential logic)
- **FPGA:** Field Programmable Gate Array (Generic Macrocells: LUT or MUX) support for high complex sequential logic

PLA & PAL

- Pre fabricated building block of many and/or gates
- Personalisation by making or breaking connections among the gates)

PLA: AND and OR are fully programmable

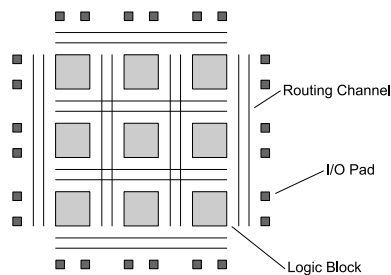
PAL: AND is programmable or is fixed fabrication



FPGA:

- Set of programmable macro cells
- Programmable interconnection Network
- Programmable Input and Output

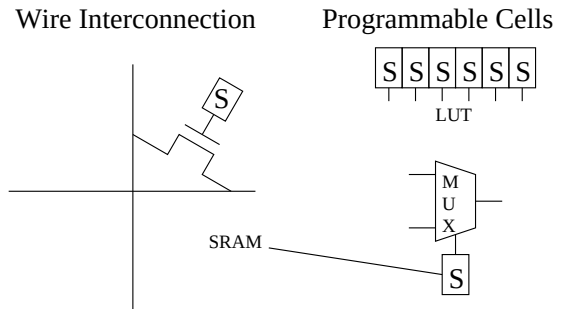
→ Fully user programmable
(Only the structure is vendor dependant)



State-of-the-Art FPGA's contain embedded IP blocs for performance efficiency (DRAM, CPU, Multiplier...) these are called Hybrid FPGA's

FPGA Programming Technologies:

SRAM: (XILINX)



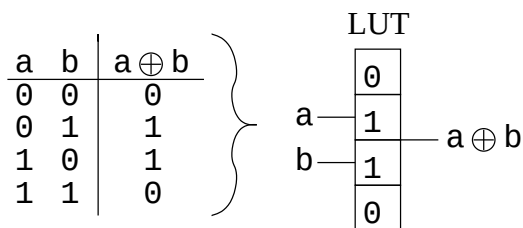
Antifuse: (ACTEL)

Antifuse presents normally high impedance state and can be fused into low impedance state by a high programming voltage.

- + Small area
- + Lower parasitics
- + No information loss when power off
- No reprogramming

LUT Function Generator:

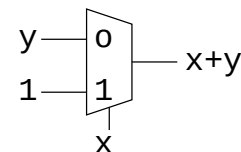
A k input LUT can implement 2^{2^k} different functions and has 2^k SRAM cells.



MUX function Generator:

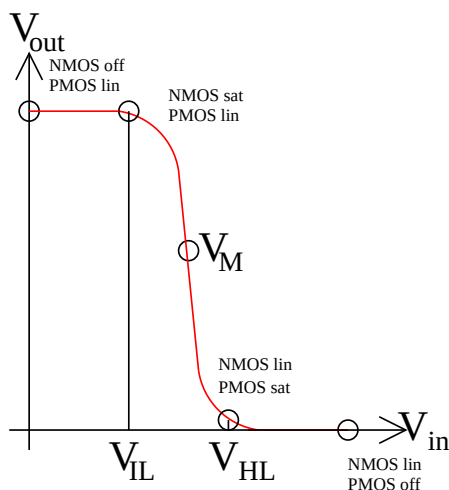
Using Shannon's Expansion Theorem allows to implement functions with multiplexers. (Functions with negation of both input variables are not realizable 12/16)

$$f(x_1, \dots, x_n) = x_i \cdot f(x_1, \dots, 1, \dots, x_n) + \overline{x_i} \cdot f(x_1, \dots, 0, \dots, x_n)$$



6 Circuit Techniques:

The Real Inverter:



Properties: $V_{OH} \equiv \text{logic 1}$

$V_{OL} \equiv \text{logic 0}$

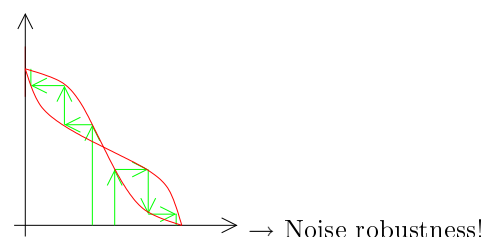
if:

$$V_{in} \leq V_{IL} \rightarrow V_{out} = V_{OH}$$

$$V_{in} \geq V_{HL} \rightarrow V_{out} = V_{OL}$$

else: Degradation!

Solution: Regenerative Property Series connection of an even count of inverters lead to a regeneration of the signal.



Complementary MOS Logic:

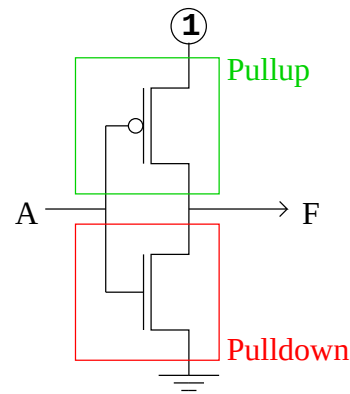
A complementary CMOS logic consists of a pullup and a pulldown network concerning a defined output. Pullup and pulldown have following dualism::

$$F^{ON} = \overline{F^{OFF}}$$

A parallel connection in PDN is equivalent to a serial connection and vice versa.

- Only inverting functions
- Implementation contains redundancy
- No static current because F is either connected to V_{dd} or GND .
- Logic behavior independent of dimension
- large SNR

CMOS Inverter:

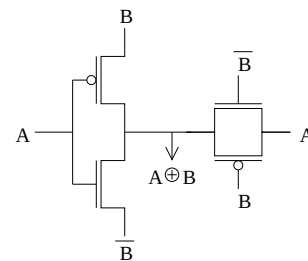


Fanin of n requires $2n$ Transistors
(n Ntype + n Ptype)

Passtransistor Logic:

- Circuit is built up of transmission gates
- Problem: level degradation of NMOS-transistors and PMOS-transistors
- Reduction of area by use of only NMOS-transistors
→ A level restorer is needed! (Inverter and a PMOS-pullup transistor)

XOR with Passtransistor Logic:



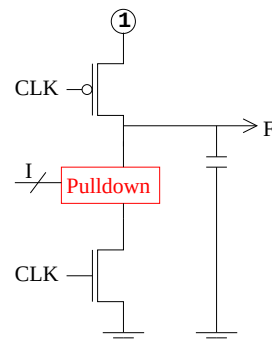
Dynamic CMOS Logic: Dynamic CMOS logic relies on temporary storage of signal values on a capacitance.

- Only implementation of a PUN or PDN
- No static power consumption
- Clock required, two phases:
Precharge: CLK=0
Evaluation: CLK=1
- High switching speed

Problem:

Cascading: 1→0 Transition causes a 1-level degradation in following gate. Solution: insert Inverters at input and outputs (Domino Logic)

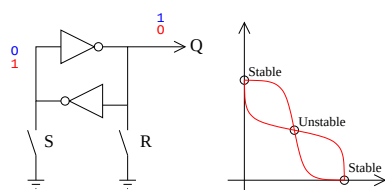
Example:



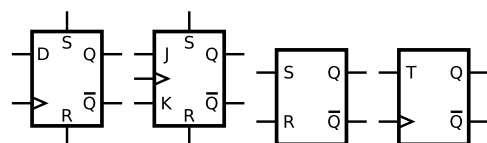
Only $n + 2$ transistors required with 2 inputs.

7 Sequential Circuits:

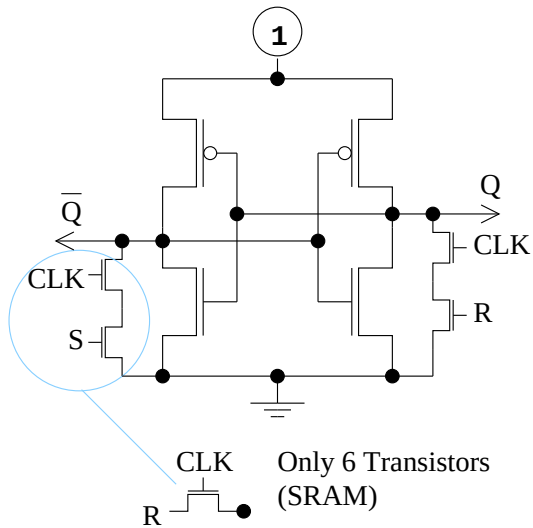
Storage Mechanism: Positive Feedback



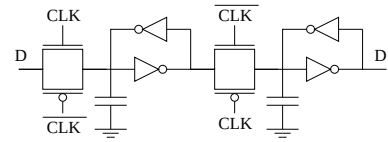
Different Types of Flip-Flops



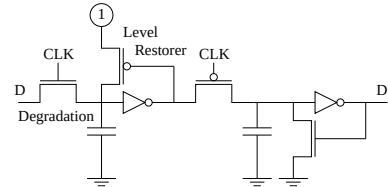
CMOS Implementation: (SR-FF)



Charge based Storage Technique: (D-FF)

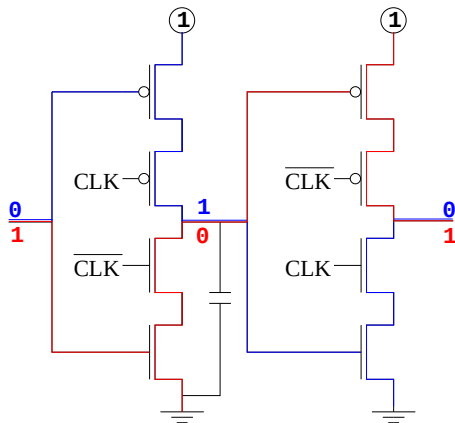


Optimization: Remove Feedback and use pass transistors. → Problem: level degradation, overlapping of CLK and $\overline{CLK}$ ($D \rightarrow D'$)



Solution: Use NMOS and PMOS pass transistor and a level restorer.

C²MOS

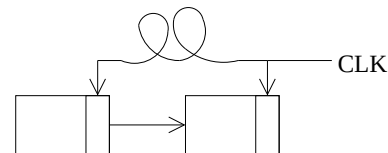


Works even if both clocking phases are overlapping

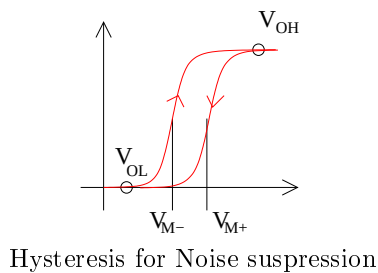
Flip Flop Delays:

- t_{Setup} : minimum time data stable before clock
- t_{Hold} : minimum time data stable after clock
- t_{pFF} : time that FF needs to have stable data on output

Clock Skew:



Schmitt Trigger:



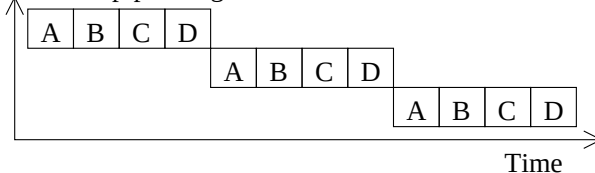
Multivibrators: Flip Flop Delays:

- *Bistable* 2 stable states (FF, ST)
- *Monostable* 1 stable state (pulse generator D-FF with XOR)
- *Astable*: No stable states (Oscillator odd series of Inverters)

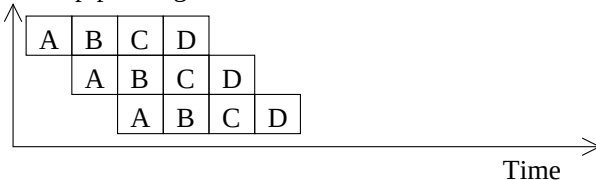
Pipelining:

Efficient technique to increase throughput in streaming based applications (audio, video...)

Without pipelining:

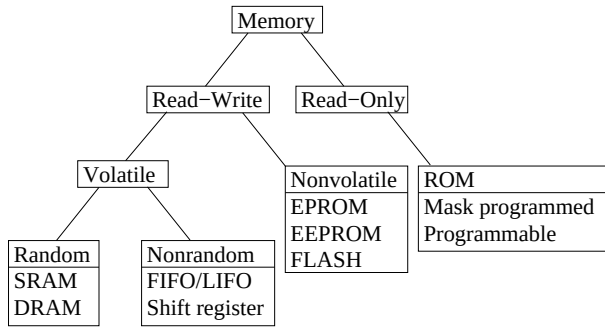


With pipelining:

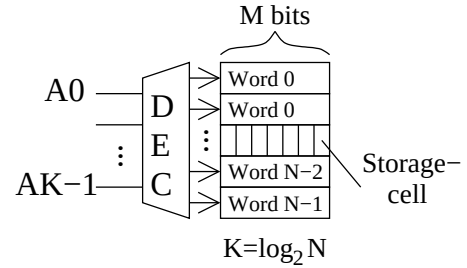


8 Memory:

Memory Classification:



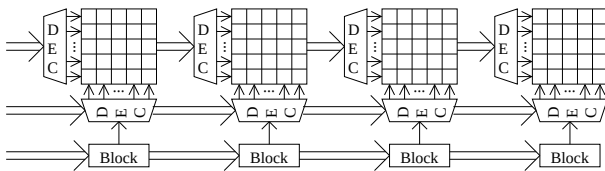
Address Decoder:



A address decoder reduces the external address signals to $k = \log_2(N)$

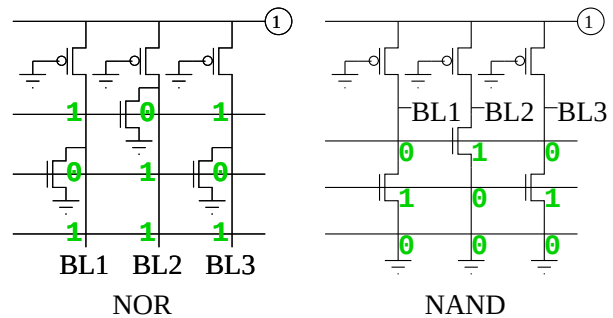
Two Stage Decoder:

Row decoder: select word line with multiple words
Column decoder: select memory word.



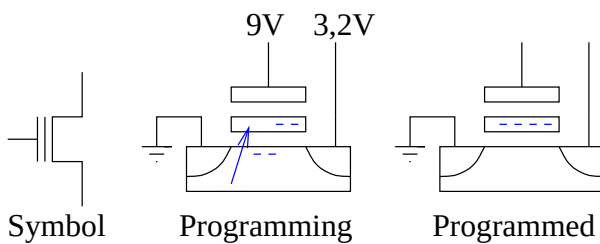
Powersaving due to activating only the needed block.
 Shorter wired within each block.

NOR and NAND ROM:



NOR: WL active = 1
 NAND: WL active = 0

Electrical Erasable Programmable ROM: (EEPROM ~ FLASH)

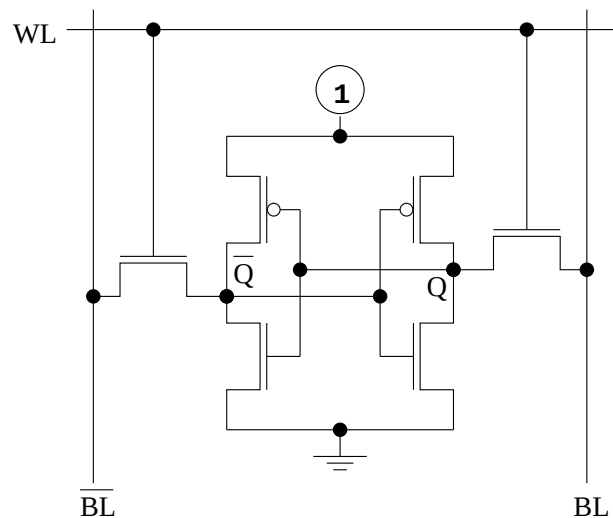


Programming: High programming voltage, electrons accumulate on the floating gate. By removing the programming voltage the electrons are trapped in the floating gate $\rightarrow V_{TH}$ is increased.

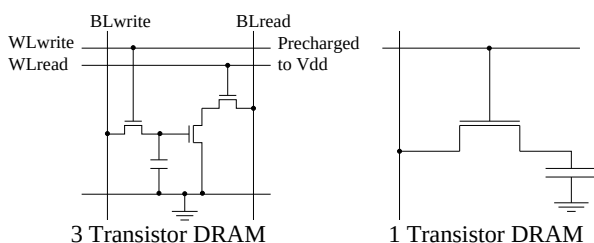
Reading: Reading the Gate with 1.8V: the transistor remains switched off due to increased V_{TH}

Erasing: UV-Light (electrons flow back) or high V_{DG} electrons tunnel to drain (Dowler Nordheim effect)

SRAM:



DRAM:



3-DRAM:

Write : Capacitor is charged via BLwrite.

Read : BLread is precharged to Vdd, dependant on capacitor BLread is discharged

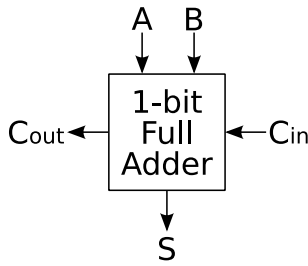
1-DRAM:

Write: voltage at capacitor is reduced by V_{TH} of MOSFET. Solution: word line boost

Read: Destructive Reading: information is destroyed during reading due to charge sharing between capacitor and bit line capacity. There are also leakage currents: refresh mechanism necessary.

9 Arithmetic Modules:

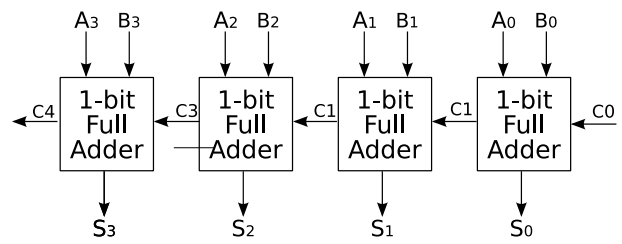
Fulladder:



$$S = (a \oplus b) \oplus c_{in}$$

$$c_{out} = \underbrace{a \cdot b}_{\text{generation}} \quad c_{in} \cdot \underbrace{(a \oplus b)}_{\text{propagation}}$$

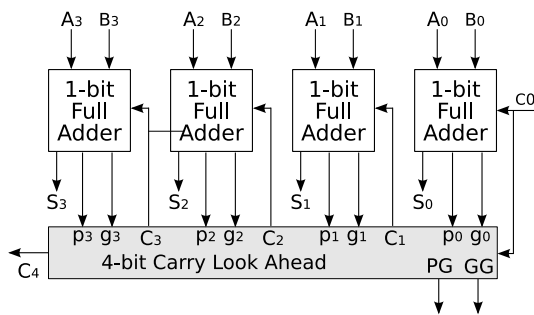
Ripple Carry Adder:



Carry 'ripples' through the adders. Problem: critical path from C_0 to C_4 . To shorten critical path in carry chain invert all inputs and outputs. (Reduces count of inverters)

Carry Look Ahead Adder:

Logic block which calculate the carries for every adder:



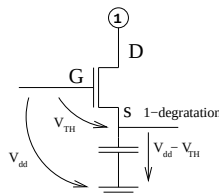
- Large Fanin/Fanout
- Area grows progressively with N

Multiplier:

$$X \cdot Y = \sum_{i=0}^{m-1} \sum_{j=0}^{n-1} x_i \cdot y_j \cdot 2^{i+j}$$

10 Miscellaneous:

Level Degradation: Example



Switch a '1' with NMOS. At the beginning the conductor is a short-circuit and $V_{DS} = V_{dd}$. After a while the conductor reaches the Voltage greater $V_{dd} - V_{th}$ so $V_{GS} < V_{th}$ and the Transistor is open.

Velocity Saturation:

$$v_x = \mu \cdot \frac{V_{DS}}{L} = \mu \cdot E_x$$

Mos Capacitys:

